UDC 681.03

J. Bača, Š. Korečko, J. Porubän, P. Václavík

DIDACTIC VERSION OF PROGRAM SYSTEM FOR SYNTHESIS AND DIAGNOSTICS OF LOGIC CIRCUITS

The Contribution deals with the Internet application of the program system for the synthesis and diagnostics of logic circuits. Internet application contents description of basic notion, theoretical principles and procedure from area of synthesis and diagnostics of logic circuits. This system comprises also programs for solution of logic circuit synthesis and diagnostic tasks. These programs can run in automatic, demo, didactic and test mode. The evaluation of student answers in didactic and test mode are saved to database, which allows analyzing by students or questions. Also the universal virtual learning environment architecture based on this program system is introduced.

Introduction

few years information А aqo, technologies have begun to apply in pedagogical process area. The first applications have been used for pedagogical process evidence and for computer-aided teaching. Later, these ones have led to development of virtual universities and complex virtual learning environments where the pedagogical process is realized through the internet.

In the next chapter the Program system for synthesis and diagnostics of logic circuits (SDLC System) is presented. SDLC System is coming out from the principles described in [1; 2; 3] and also from learning environment [4]. This system is realized as complex Internet application and provides the virtual learning environment for subjects "Logic Systems" and "Diagnostics and Reliability of Logic Systems" which are lectured at our department.

In the third chapter the universal virtual learning environment architecture based on our experiences from the development of the SDLC System is introduced.

1. The SDLC System

The development of this system has started in year 2000 [5]. First modules of the SDLC System were realized in diploma thesis [6; 7; 8; 9; 10; 11; 12; 13; 14; 15; 16; 17; 18; 19]. Detailed description of these modules as well as the description of the synthesis and diagnostics process can be found in [5; 20]. Another four modules, with multi-lingual support, have been added this year. Currently, after two years of development work, the SDLC system consists of 18 modules and the size of the system is 40MB.

Next sections describe the parts of the system. This description is not oriented to technological system design but to aspects important for the pedagogical process.

1.1. Structure of the SDLC System. The structure of the SDLC System is shown on Figure 1. After authentication of a user (student or instructor) the start page is shown. This page includes the hyperlinks to modules and the short description of each module. It also allows instructors to see and analyze the results of the didactic tests made by the students. Each module explains one stage of the process of synthesis and diagnostics of logic circuits. It also includes the didactic tests to verify student knowledge about given stage. The results of these tests are saved in the database and can be accessed by instructors for analysis and evaluation of students. The SDLC system also includes tools for the administration of databases.

1.2. Modules. The SDLC System has modular structure. This allows expanding or reducing the system quite easily — by adding or removing the modules. It also reduces the downloading time and memory requirements, because not the whole system is downloaded but only the required module. Each module consists of three basic elements: index

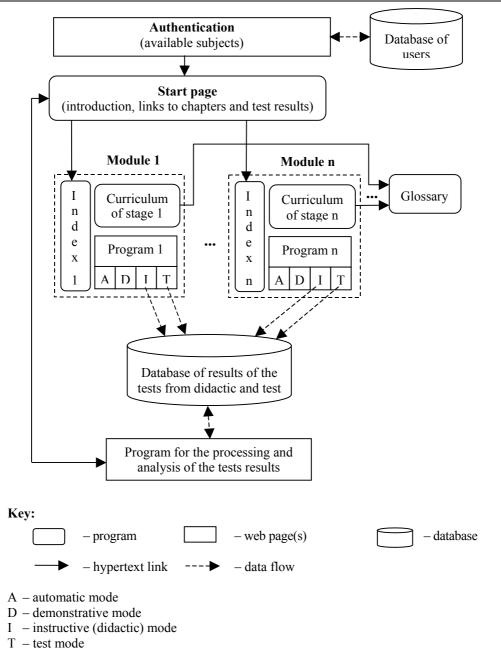


Fig. 1. The structure of the SDLC System

page, curriculum pages and the demonstration program.

1.3. Index page. This page serves as the introduction to the given module. It includes basic information about module, its authors as well as the menu with hyperlinks to the other parts of module – curriculum pages and program.

1.4. Curriculum pages. The theory of the given stage of the synthesis and diagnostics process is explained on these pages. It comprises terms, facts, principles, rules, methods and explanation of the algorithm of the given stage.

Each curriculum page explains one part of the theory (one chapter) and is divided into three areas (Fig. 2):

• *Text* — title and text of the chapter. The text includes links to the glossary and to multimedia resources (pictures, animations, etc.). The glossary is web page with alphabetically ordered definitions of terms used in the explained area. The glossary is common for all modules.

• *Visualization area* — after clicking the link in the text the corresponding picture, animation or the glossary with

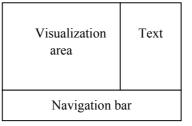


Fig. 2. Design of the Curriculum page

definition of the corresponding term is displayed in this area.

• *Navigation bar* — includes buttons for navigation through the chapters of the curriculum.

1.5. Program. The program implements the algorithm of the given stage of the process of synthesis and diagnostics of logic circuits. It is realized as the Java applet and can run in automatic, demonstrative (learning), didactic (instructive) or test mode. The automatic mode is used for the process of synthesis and diagnostics itself and the other three modes are used for the pedagogical purposes.

In *automatic mode* the input data are written in build-in editor or are loaded from the input file. Then the algorithm of the given stage is executed and the results of the execution are displayed. The results are saved into the output file, if it is required. The input and output files are text files so they can be written or changed using any text editor. The syntax or these files is simple and easy to understand. The output file of one program is the input file of another program (from another module), which realizes the next stage of the process of synthesis and diagnostics.

In *demonstrative mode* the algorithm is executed step-by-step and every step is explained. The execution is stopped after each step to allow the student to see the temporary results and the description of the step. The execution continues after clicking the "step" button. Student can also skip one or more steps or terminate the execution.

In *didactic mode* students can test their knowledge about the given stage by answering the questions. There are two types of questions — theoretical and

practical ones. Theoretical questions verify the knowledge of the curriculum. Practical questions verify the knowledge of the algorithm. These questions are put to a student during the execution of the algorithm — instead of the description there is a question after each step. When the answer is wrong the student can answer again. After three unsuccessful attempts the right answer is displayed. Students need not to answer all questions — they can skip one or more questions. The results of the test (number of questions, number of right answers, time needed to answer the questions, etc.) are saved into the database.

The *test mode* is alike the didactic mode but student cannot correct the wrong answer and no question can be skipped. The questions are selected randomly so no students have the same questions. The results of the test are saved into the database and are used for the evaluation of the student knowledge about the given stage.

2. Universal Virtual Learning Environment Structure

In this chapter the universal virtual learning environment architecture based on the SDLC System is described.

Fig. 3 depicts universal virtual learning environment architecture. This architecture presents user part of the new universal system. This one is divided into two places. The first place is client side. Simple system availability is performed using web browser with 128-bit SSL present support. At the time. the computer security is one of basic element of each program. Client side is divided to some levels. First level is available for each web browser user. It just comprises the introduction about this system and it is possible to login to the system. At the second level (if you enter to the system successfully) you can select one of the available subjects. Availability of subjects depends on your permission. Moreover, you can choose your personal setting where is possible to set language version (internationalization support), change a password, etc. If you choose some subject then the particular subject module will be available. Modules are the part of third level.

The module consist of:

• index — chapter outline, chap-

ters list, basic characteristics of a problem;

• *curriculum part* — the theory of a subject chapter, the explanation of the solution of a problem, test questions;

• program — is narrowly adherent to curriculum part. It comprises animations, pictures, video, Java applets, etc.;

• *navigation bar* — the panel for navigation *curriculum part* (the *program* is controlled by separate navigation panel). It is hidden in the schema;

• mode selection (A,D,I,T) — this is probably the most important system part. The explanation of these modes has been presented in previous chapter;

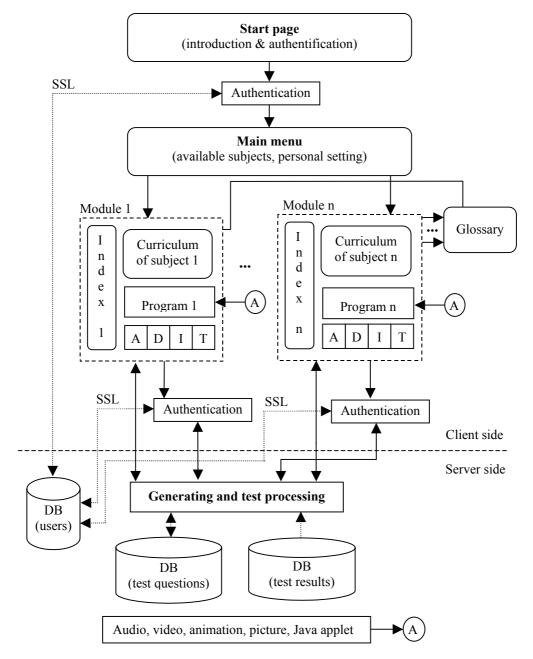


Fig. 3. Universal virtual learning environment architecture

• *glossary* — each module has individual glossary (one glossary for one subject).

Server side is used to serve data (theory, glossary, animation, picture, test, etc.) to a client. It concerns oneself to:

• *authentication* — this is important in two cases. First case is user login to system. Second case is user login to test examination;

• *permission* — it provide access to the data according to assigned permission;

• *test generating* — this is one of the most important parts of education process. Test results are used to enhance the instructional process in variety of ways. Questions selection are parameterized over the test area, complexity, score, etc.;

• *test processing* — completed test and test result is saved to database. The test result is given to the user;

• data administration — this part is used to manage the temporary and permanent records.

Conclusion

SDLC System has been developed at Department of Computers and Informatics at the Technical University of Kosice. The main aim is to create system for arbitrary subject where user has the opportunity to make decision to work in any mode defined above. Multilingual (international) support is one of the main aims. It leads to using this system by students in other countries through the internet.

New (universal) analysis and design of the system are first steps before implementation. However, the precision of these steps processing is very important for future work. Our first design presented in this paper is oriented just to user view. It is possible that this architecture design will be a bit adjusted, taking into account the experiences from the development and use another of e-learning projects [21]. Loading data to the system and their administration (user assigning, setting user permission, etc.) are over the scope of this paper.

Future work will be oriented to practical realization of this architecture where the correctness of the design will be verified.

- Bates B., Leary, J. J. Teleeducation Environments: Issues of Learning Styles // Proc. ISTEP 2000, Košice, Slovakia, 22-24 March, 2001. — P. 39-45.
- 2. *Messick S.* Individuality in Learning. —San Francisco: Jossey-Bass, 1976.
- 3. *Kolb, D.A.* Experiential Learning. NJ: Prentice Hall Englewood Cliffs, 1984.
- Multimedia Virtual Campus / J.L. Gonzáles-Sanchez, A. Gazo-Cervero, J.L. Gordo-Rivera, M. Sanchez // Proc. Advances in Multimedia and Distance Education ISIMADE99. — Baden-Baden (Alemania), 1999. — Aug.
- Bača J. Exploitation of application programs in teleeducation // Intern. Symp. on Telemedicine and Teleeducation in Practice. — Košice, 22-24 March 2000. Košice: Elfa, 2000.
- 6. Čech A. Determination of the forcing and output functions: Semestral project. — Košice: Department of Computers and Informatics, Technical University of Košice, 2001.
- Grušovský G. Decomposition of logic circuits into the modules: Diploma thesis. — Košice: Department of Computers and Informatics, Technical University of Košice, 2001.
- 8. *Gužík P.* Determination of the tests of logic circuits by the Boolean difference: Diploma thesis. Košice: Department of Computers and Informatics, Technical University of Košice, 2001.
- Hollý P. Determination of the SNDF by the Qiune-McCluskey's algorithm: Diploma thesis. — Košice: Department of Computers and Informatics, Technical University of Košice, 2001.
- Jurcák P. Determination of the tests of logic circuits by the critical path method: Diploma thesis. — Košice: Department of Computers and Informatics, Technical University of Košice, 2001.
- 11. *Korečko Š.* The Automatic Full Test Generation for Digital Circuits with the Modular Structure: Diploma thesis. Košice: Department of Computers and Informatics, Technical University of Košice, 2001.
- 12. *Krištofičová B.* Determination of the irredundant NDF by the Qiune-McCluskey's algorithm: Diploma thesis. — Košice: Department of Computers and Informatics, Technical University of Košice, 2001.
- Kubalec M. Generation of the tests of logic circuits using the D-algorithm, Diploma thesis. — Košice: Department of Computers and Informatics, Technical University of Košice, 2001.

- 14. Nehila M. Reduction of the states of the finite state machines: Diploma thesis. — Košice: Department of Computers and Informatics. Technical University of Košice, 2001.
- Pulen T. Determination of the irredundant NDF by the Petrick method: Diploma thesis. — Košice: Department of Computers and Informatics, Technical University of Košice, 2001.
- 16. *Skurka S.* Abstract synthesis of the sequential logic circuits: Diploma thesis. Košice: Department of Computers and Informatics, Technical University of Košice, 2001.
- 17. Štoffan O. Database for the evaluation of the results of didactic tests: Diploma thesis. Košice: Department of Computers and Informatics, Technical University of Košice, 2001.
- Weber T. Fault location of the logic circuits by independent test: Diploma thesis. — Košice: Department of Computers and Informatics, Technical University of Košice, 2001.
- Zaťko Š. Optimal coding of the states of synchronous sequential logic circuits: Diploma thesis. — Košice: Department of Computers and Informatics, Technical University of Košice, 2001.
- 20. *Bača J.* Internet application of program system for synthesis and diagnostics of logic circuits // Proc. of Czech and Slovak education

workshop, Herl'any, 25–26 Oct. 2001. Košice: Elfa, 2001.

 Friesen K., Schmitz H. Managing the development of an e-learning product-Applying software engineering techniques in an academic environment // Proc. World Congress of Networked Learning in a Global Environment, Berlin, Germany, May 1-4, 2002. — Berlin, 2002.

Date received 26.08.03

About authors

Dr. Ján Bača, Dr. Štefan Korečko,

Dr. Jaroslav Porubän,

Dr. Peter Václavík

Technical University of Košice Department of Computers and Informatics, Letná 9, 041 20 KOŠICE, Slovak Republic

E-mail: jan.baca@tuke.sk,

stefan.korecko@tuke.sk, peter.vaclavik@tuke.sk, jaroslav.poruban@tuke.sk